Enabling High Aspect-Ratio Interconnects for Advanced Packaging of MEMS and Sensors

A breakthrough metal atomic layer deposition solution for enabling deep vias with aspect ratios exceeding 30:1

Executive Summary

The miniaturization and increased functionality of modern electronic devices demand advanced packaging solutions with higher interconnect densities. However, as aspect ratios of interconnects increase, traditional deposition methods face significant limitations. This white paper presents Forge Nano's breakthrough thermal atomic layer deposition (ALD) solution for metal barrier/seed applications on high aspect ratio vias, enabling unprecedented conformal coating in structures with aspect ratios exceeding 30:1.

Our innovative approach delivers:

- Complete via metallization solutions for both silicon and glass applications
- Superior conformal coverage compared to traditional PVD/CVD methods
- Enhanced device reliability and reduced defect rates
- New possibilities for device architecture and design freedom

Introduction: The Interconnect Challenge

Scaling interconnects to increase device density remains a critical bottleneck for advanced packaging and heterogeneous integration strategies. For microelectromechanical systems (MEMS), interconnect depths are often dictated by device requirements - such as the need for a tall device layer to provide sufficient proof mass for desired sensitivity.

While copper (Cu) continues to be the interconnect metal of choice, its implementation in high aspect ratio structures presents significant challenges:

1. Uniform diffusion barrier application throughout the via
2. Consistent metal seed layer deposition for smooth, dense Cu electroplating
3. Prevention of voids and defects during electrodeposition

The state-of-the-art processes for high-quality metal barrier and seed films typically rely on line-of-sight techniques like physical vapor deposition (PVD). Unfortunately, these methods become ineffective at aspect ratios above 10:1—sometimes as low as 4:1—especially when dealing with complex geometries like undercuts.

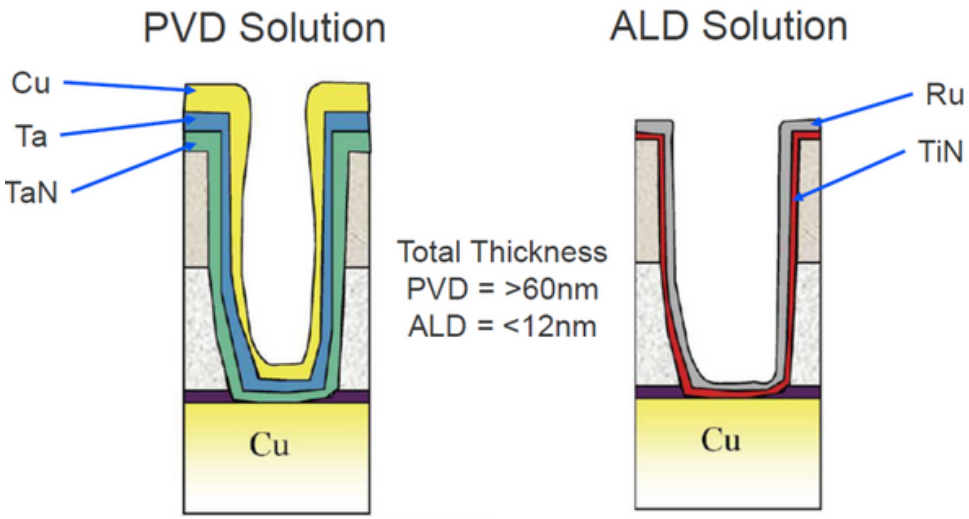

Figure 1: Comparison of traditional PVD deposition (left) showing poor conformality versus ALD solution (right) from Kim, H. et al., Surf. Coat. Tech., 200, 3104-3112 (2006).

When traditional deposition methods fail to provide uniform coverage, the consequences include:

- Insufficient adhesion between layers
- Inconsistent seed layer thickness
- Voids in Cu lines
- Vertical thickness gradients leading to "pinch-off" at the via top
- Device failure due to high line resistance or dielectric breakdown

Forge Nano's ALD Metal Barrier/Seed Solution

Atomic layer deposition (ALD) represents the ideal approach for achieving conformal metal films for both Cu diffusion barrier and electrodeposition seed applications in high aspect ratio structures. Forge Nano has developed a complete thermal ALD solution demonstrated to be effective on structures with aspect ratios exceeding 30:1.

Technology Innovation

While ALD metals have been explored for barrier/seed applications, their adoption in production environments has been limited due to:

- Slow deposition rates
- Poor precursor efficiency
- Reliance on plasma enhancement (which limits aspect ratio capability)

Forge Nano's proprietary ALD^{x} toolset overcomes these limitations with:

- Proprietary fast dosing valves with 1ms actuation times
- Unique chamber design optimized for rapid purging
- All-thermal catalyzed processes for unlimited aspect ratio capability

Applications

- Interconnects for MEMS and sensors
- Through silicon vias (TSVs)
- Through glass vias (TGVs)
- Heterogeneous integration
- Advanced packaging
- High-frequency devices

The Complete Stack Solution

Our comprehensive approach offers tailored solutions for both silicon and glass via applications:

For Silicon Vias:

1. **Dielectric Barrier**: Proprietary thermal SiO_2 ALD CRISP with high deposition rate and excellent dielectric properties
2. **Cu Diffusion Barrier**: Low-temperature (300°C) TiN thermal ALD process
3. **Cu Seed Layer:** Conformal ruthenium (Ru) ALD film

For Glass Vias:

A simplified stack utilizing:

1. Thinner TiN ALD to promote adhesion and Ru nucleation
2. Ru ALD as the Cu seed layer

Film Properties At A Glance

ALD Film	Deposition Rate	Density	Resistivity	Dielectric Breakdown
SiO_2	10 nm/min	2.3 g/cm³	-	>12 MV/cm
TiN	1 nm/min	5.0 g/cm³	500 μΩ·cm	-
Ru	0.33 nm/min	12.0 g/cm³	<20 μΩ·cm	-

Stack Performance

When compared to traditional PVD stacks (Ti/W adhesion layer and Cu seed), our ALD solution shows dramatic improvements.

In 4:1 Aspect Ratio Blind Si Vias:

✓ Forge Nano ALD Solution

Delivers uniform Cu electrodeposition throughout the entire via structure with excellent adhesion

✗ Traditional PVD Solution

Shows voids at via bottoms due to adhesion failures and vertical non-uniformity with "bread loafing" at the top, eventually leading to pinch-off

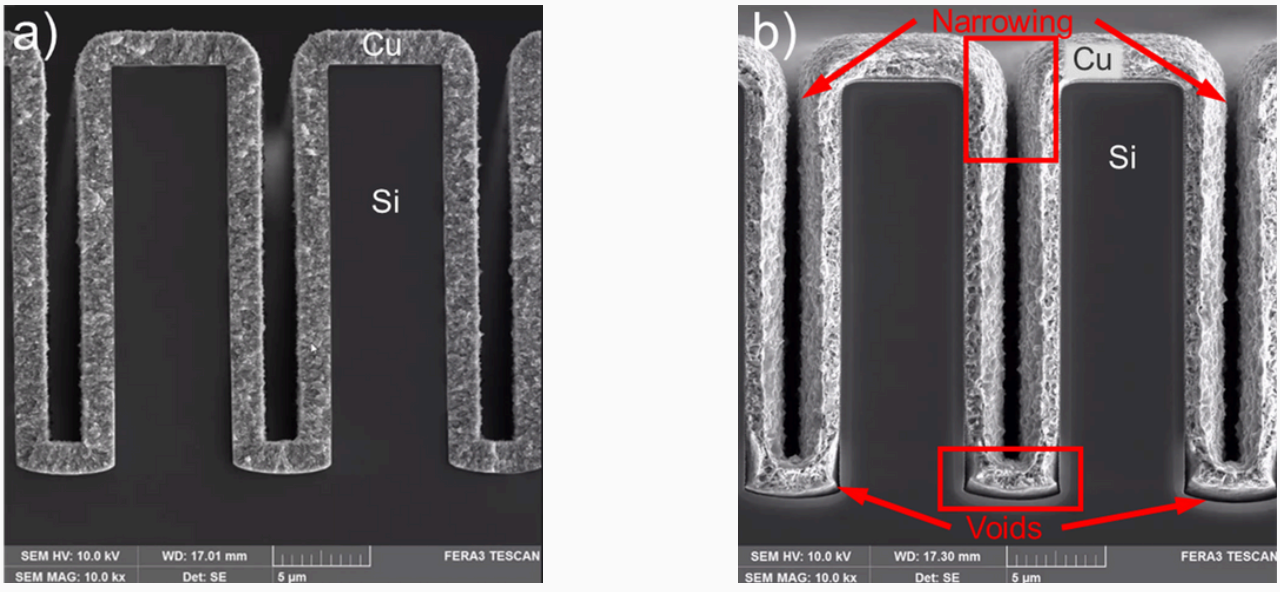

Figure 2: SEM micrographs of Cu electrodeposited in 4:1 aspect ratio Si vias that have a) the ALD stack described and b) PVD Ti/W adhesion layer followed by a PVD Cu seed layer. There are obvious failures in b). Voids have occurred at the bottom from adhesion failure of the Cu electrodeposition and narrowing, eventually leading to pinch off, has started at the top of the vias. Failures are shown in boxes and with arrows in b).

In 10:1 Through Glass Vias:

Our simplified stack for TGVs also offers high conformality of both ALD film and subsequent Cu electroplating.

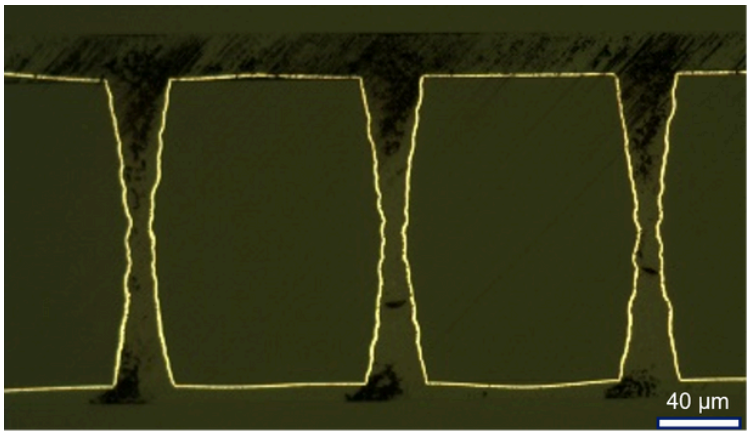

Figure 3: 10:1 aspect ratio TGVs coated with a TiN/Ru ALD stack then electroplated with Cu. The electrodeposited Cu adheres well to the Ru seed and nucleates conformally both on the trench sidewalls and the top and bottom of the wafer.

Key Benefits

- Conformal coating in ultra-high aspect ratio structures (>30:1)
- Eliminates voids and pinch-off in electropated Cu
- Enhances device reliability and yield
- Enables new device architectures
- Production-worth throughput rates

Cu ECD Nucleation Progression

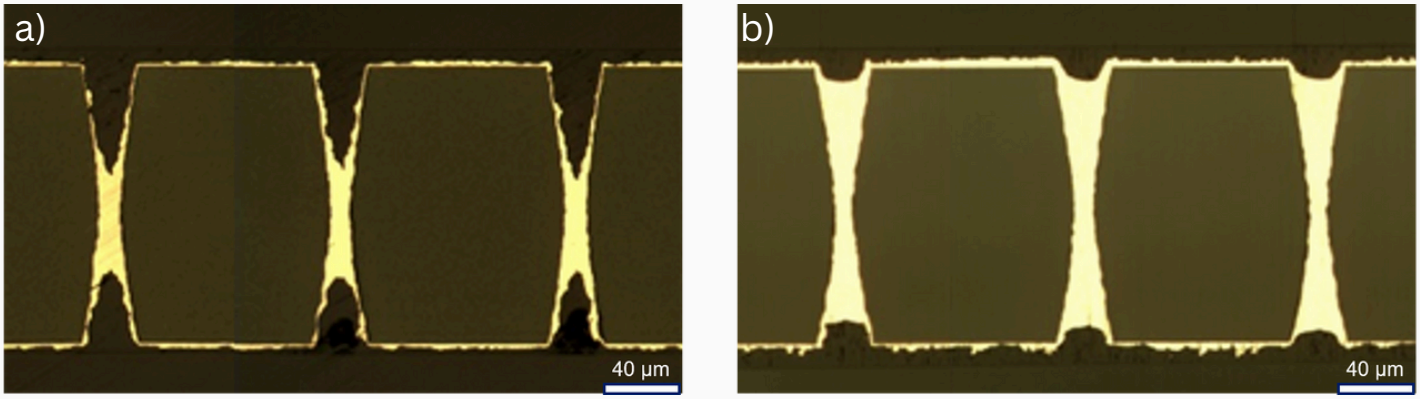

Figure 4: As electrodeposition of Cu proceeds on our ALD in TGVs, it starts in the middle of the via (a), then creates a conformal and symmetric fill (b), free from any voids or bread-loafing as seen with PVD solutions.

Scalable Solutions

Single Wafer Quality at Batch Throughputs

Forge Nano's ALD^{x} toolset brings traditionally sluggish ALD processes to viable manufacturing throughputs. In the TEPHRA™ cluster platform, the following production throughputs are achieved for our metal/barrier seed stack:

- Single chamber configuration: ~0.25 wafers/hour
- Dedicated chamber for each process: ~0.75 wafers/hour
- Fully outfitted 8-sided TEPHRA platform: >2 wafers/hour

TEPHRA™ 200mm Cluster Platform

Forge Nano's TEPHRA™ ALD system delivers industry-leading deposition rates with unmatched precursor efficiency for metal ALD films.

Learn more about TEPHRA™ -->

Our Other ALD Solutions

- Anti-stiction coatings
- Gap fill
- High-*k* dielectrics
- Moisture barriers
- Passivation films

NEW

In Development: Panel Form Factor Capable

As the advanced packaging industry seeks more cost-effective solutions, Forge Nano ALD^{x} processes not only enable interconnect scaling, but also form factor scaling. Our catalyzed processes are well-suited to enable the transition from wafers to next-generation panel designs.

Note: TEPHRA™ is a wafer-only tool, panel form factors are processed in different equipment.

Conclusion: Enabling Speed and Power of Next-Generation Devices

Forge Nano's thermal ALD barrier/seed solution enables reliable metallization of high aspect ratio vias that are simply not possible with traditional deposition methods. With demonstrated success in structures up to 30:1 aspect ratio, our technology unlocks new possibilities for:

- Higher density interconnects
- Novel device architectures
- Improved device performance
- Enhanced manufacturing yields
- Reliable heterogeneous integration

As interconnect scaling continues to be a critical challenge for advanced packaging, our ALD approach provides a production-worthy solution that extends well beyond the limitations of conventional techniques.

For demo requests, sales inquiries or more information on our ALD solutions and equipment, please message

Tyler Myers, Ph.D
Product Marketing Manager
tmyers@forgenano.com

or contact us here.

About Forge Nano

Forge Nano is designing the future of material change. With proprietary ALD^{x} technology, Forge Nano enables semiconductor fabs to conformally coat 200mm wafers for encapsulation, passivation, high-κ dielectric and metal barrier seed applications with single wafer quality at batch speeds and unprecedented chemical efficiency. Forge Nano's team of scientists have worked with an expansive portfolio of commercial partners to develop custom solutions to meet any need at any scale, from small-scale R&D and laboratory work to large-scale, high-volume production.

Learn more at www.forgenano.com.